

Claims

- [c1] A memory device, comprising:
- a memory cell array having a multitude of memory cells, first and second bitlines, and first and second wordlines, each of said memory cells being coupled to one of said first bitlines, one of said second bitlines, one of said first wordlines, and one of said second wordlines;
 - each of said memory cells being accessible through one of said first wordlines and one of said first bitlines by an external port and being accessible through one of said second wordlines and one of said second bitlines by an internal port;
 - said external port being connected to input terminals to receive input signals in order to select one of said memory cells for an external data access; and
 - a refresh control unit generating refresh control signals to access one of said memory cells to perform a refresh of the respective one of said memory cells through said internal port.
- [c2] The memory device according to claim 1, wherein each one of said memory comprises:
- a first selection transistor coupled to one of said first wordlines and one of said first bitlines;
 - a second selection transistor coupled to one said second wordlines and one of said second bitlines; and
 - a storage node connected to said first selection transistor and said second selection transistor.
- [c3] The memory device according to claim 2, wherein each one of said memory comprises:
- a storage transistor having a drain/source path and a gate terminal, said drain/source path being connected to said first and said second selection transistors; and
 - said gate terminal being connected to a reference potential.
- [c4] The memory device according to claim 1, wherein said external port is connected to input terminals designed to receive one of an address signal, a

signal determining a read or a write operation, a data clock signal, and a device select signal.

- [c5] The memory device according to claim 4, wherein said internal port is hidden from said address signal, said signal determining a read or a write operation, and said device select signal.
- [c6] The memory device according to claim 1, comprising:
a first bank of sense amplifiers, wherein each one of said first bitlines is connected to one of said sense amplifiers of said first bank;
a column decoder, wherein an individual one of said sense amplifiers of said first bank can be selected to perform one of data read to an external terminal;
and
data write from an external terminal.
- [c7] The memory device according to claim 6, comprising:
a second bank of sense amplifiers, wherein each one of said second bitlines is connected to one of said sense amplifiers of said second bank, and wherein multiple of said amplifiers are selected to perform a refresh of a row of memory cells.
- [c8] The memory device according to claim 1, comprising:
a first clock terminal to receive a system clock signal to synchronize external data input and output;
a second clock terminal to receive a reference clock signal; and
a synchronization circuit to output a refresh clock signal which is synchronized to one of said system clock or said reference clock signals.
- [c9] The memory device according to claim 8, comprising:
a refresh address counter to generate row addresses of rows of memory cells to be refreshed, said address counter being controlled by said refresh clock.
- [c10] The memory device according to claim 1, comprising:
a contention detection circuit, said contention detection circuit receiving a row address in response to an external read or write access through said external port and receiving a refresh address for a row of memory cells to be refreshed,

said contention detection circuit suppressing a refresh, if said refresh address equals said row address.

[c11] The memory device according to claim 1, wherein said memory cell array comprises at least two blocks of memory cells, said blocks being provided with a refresh row address in parallel, said refresh control circuit generating a separate refresh enable signal for each of said blocks to perform a refresh operation for one of said blocks subsequent to a refresh operation for another one of said blocks.

[c12] A memory device, comprising:
a memory cell array having memory cells, each of said memory cells being accessible through a first port and through a second port, only said first port of said first and second ports being accessible by an external address signal to select one of said memory cells; and
a refresh control circuit designed to generate refresh control signals to refresh said memory cells through said second port.

[c13] The memory device according to claim 12, comprising:
a contention detection circuit receiving a refresh address to access a subset of said memory cells and an address to access at least one said memory cells of said subset of memory cells for an external read or write operation, said contention detection circuit suppressing a refresh operation for said subset of said memory cells.

[c14] The memory device according to claim 13, wherein a refresh operation is performed for another subset of memory cells.

[c15] The memory device according to claim 13, wherein said subset of memory cells is a row of memory cells.

[c16] The memory device according to claim 12, wherein said refresh control circuit receives a system clock signal and a reference clock signal, said refresh control circuit has a refresh address counter to provide a sequence of addresses for subsets of memory cells to be refreshed, said memory device having a normal mode and a power-down mode, wherein said refresh address counter is

controlled by said system clock signal during the normal mode and is controlled by said reference clock signal during the power-down mode.

[c17] The memory device according to claim 16, wherein said refresh control circuit comprises a synchronization circuit that synchronizes a clock signal to one of said system clock or reference clock signals in response to one of said normal or power-down modes, wherein said clock signal controls said refresh address counter.

[c18] The memory device according to claim 16, wherein said reference clock signal has a lower frequency than said system clock signal.

[c19] The memory device according to claim 12, wherein each one of said memory cells comprises:
a first selection transistor coupled to one of said first wordlines and one of said first bitlines and a second selection transistor coupled to one said second wordlines and one of said second bitlines; and
a storage node connected to said first selection transistor and said second selection transistor.

[c20] A memory device, comprising:
a memory cell array having a multitude of memory cells arranged in rows;
a first row decoder to activate one of said rows in response to an external address;
a second row decoder to activate one of said rows in response to an internal address; and
a refresh control circuit to refresh the memory cells of a row which is activated by said second row decoder.

[c21] The memory device according to claim 20, wherein said refresh control circuit comprises a contention detection circuit suppressing the refresh operation when the row to be activated by said first row decoder and the row to be activated by said second row decoder are the same row.

[c22] The memory device according to claim 20, wherein each one of said memory cells comprises a first selection transistor connected to the first row decoder

through a first wordline and a second selection transistor connected to the second row decoder through another wordline and a storage node coupled to the first and the second selection transistors.